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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,869	06/30/2000	Stephen S. Chang	042390.P8815	2389

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EXAMINER	
BANANKHAH, MAJID A	
ART UNIT	**PAPER NUMBER**
2127	4

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/608,869	Stephen Chang
Examiner	**Art Unit**
Majid Banankhah	2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 30, 2000* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-30* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. This office action in response to application filed on June 30, 2000. Claims 1-30 are presented for examination.

2. The abstract of the disclosure is objected to because it does not describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. Correction is required. See M.P.E.P. 608.01 (b).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The examiner believes that the title of the invention is broad. A descriptive title indicative of the invention will help in proper indexing, classifying, searching, etc. See MPEP 606.01. However, the title of the invention should be limited to 255 characters.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, and are rejected under 35 U.S.C. 102(b) as being anticipated by Stamm et al. (U.S.Pat No. 5,404,483).

Per claims 1, 11, and 21, Stamm teaches:

a task table coupled to a bus interface to store task entries corresponding to tasks executed by at least one processor (Fig. 7, CPU bus, and col. 4, lines 12-13); a block allocation circuit coupled to the bus interface and a cache memory to allocate blocks of the cache memory used by at least one of the tasks (Fig. 2, read allocate, write allocate, and primary cache, col. 11, lines 12-27; and a task coordinator to coordinate the tasks in response to a task cycle issued by the at least one processor (Fig. 1, 25, memory management unit, and col. 6, lines 38-47, clock generator 31).

Per claims 2, and 12, and 22, each of the task entries comprises at east one of a task status (, a task identifier (ID), a task start address, a task block size (col. 2, lines 21-35), and a task cache address (address portion of memory, col. 2, lines 21-35).

Per claims 3, and 13, and 23, the task cycle provides at least one of the task ID, a task command, the task start address, and the task block size (col. 18, lines 42-60, alternate with address cycles containing 32-bit addresses plus byte masks and data length fields; a parallel command and arbitration bus

carries a command on lines 20b, an identifier field on lines 20c defining which node is sending, and an Ack on line 20e; separate request, hold, grant, suppress and writeback-only lines are provided to connect each node to the arbiter 325).

Per claims 4, and 14, and 24, the block allocation circuit comprises:

a search logic circuit to Locate a free UNLOCK by mining througn a use of busy flags corresponding to data blocks in use in the cache memory; and a block information generator coupled to the block search logic to generate block information of a free block available for a new task, the block information including at least a block size, a block starting address, and a block ending address (col. 27, lines 55-68, continued on col. 28, lines 1-12, The primary purpose of the fill CAM 302 is to hold the addresses and other information related to memory access commands which have missed in the back-up cache so that further accesses to those cache blocks can be prevented until the cache fills are returned from memory. But the fill CAM 302 is also used to hold outstanding READ LOCK information, so that access to a locked cache block is also prevented until the corresponding WRITE UNLOCK is executed).

Per claims 5, and 15, and 25, task coordinator comprises: a task table updater to update the task table; and an address generator to generate address information to the cache memory (col. 16, lines 17-33, the writeback queue 62 can be emptied as needed **so that the other nodes of the system continue to have updated data available in system memory 12**).

Per claims 6, and 16, and 26, the task status is one of an invalid status, a shared status, and an exclusive status (col. 2, lines 4-21, Whenever processors communicate via a shared memory, it is desirable to require the processors to follow a protocol ensuring that a memory address is not written to simultaneously by more than one processor, or else the result of one processor will be nullified by the result of another processor. Such synchronization of memory access is commonly achieved by requiring a processor to obtain an exclusive privilege to write to an addressed portion of the shared memory, before executing a write operation. In a multi-processor system employing writeback caches, such an exclusive privilege gives rise to a cache coherency problem in which data written in the cache of a processor having such an exclusive privilege might be the only valid copy of data for the addressed portion of memory. A cache coherency protocol is required which permits a processor to

obtain readily the valid copy of data as well as the privilege to write to it).

Per claims 7, and 17, and 27, the task command is one of a read shared command, a read exclusive command, a write command, and a flush command (Read and Write command, col. 9, lines 15-37).

Per claims 8, and 18, and 28, the task block size corresponds to number of cache lines in one of the blocks (col. 23, lines 14-39, As fill data returns, the cache controller unit 26 keeps track of how many quadwords have been received with a two-bit counter in the fill CAM 302. If two read misses are outstanding, fills from the two misses may return interleaved).

Per claims 9, and 19, and 29, the bus interface is one of a processor bus interface and a multi processor bus interface (Fig, 1, CPU 28, and CPU 28, and bus interface 11).

Per claims 10, 20, and 30, the cache memory is one of an internal cache and an external cache with respect to the at least one processor (col. 5, lines 3-18, When fetching instructions or data, the CPU 10 accesses an internal or primary cache 14, then a

larger external or backup cache 15).

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Majid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington. VA, Six Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses to the Examiner.

All Formal or Official Faxes must be signed and sent to either (703) 308-9051 or (703) 308-9052. Official faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District

of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the office, e.g., Finance Division for fee charging, etc.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Majid Banankhah

June 2, 2003

MAJID BANANKHAH
PRIMARY EXAMINER